AMENDMENTS TO THE CLAIMS:

Please cancel claim 10, without prejudice. Kindly amend claims 2, 3, 9, 11, 12, 13, 14, 16 and 17, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (previously presented): A stacked semiconductor storage device comprising, in combination, a lower chip and an upper chip superimposed on a substrate, said semiconductor storage device further comprising:

a wiring substrate having wiring patterns thereon, interposed between and in direct contact with both said lower chip and said upper chip, for relaying electric connection between bonding pads on said upper chip and bonding pads on said substrate, wherein the bonding pads on said upper chip are arranged in a line running perpendicular to a line of bonding pads on the substrate;

wherein said upper chip has an upper and a lower surface, said lower surface facing said substrate; and

wherein the bonding pads on said upper chip that connect to the bonding pads of said substrate are disposed on the lower surface of said upper chip.

Claim 2 (currently amended): A stacked semiconductor storage device as claimed in claim 1, wherein said wiring pattern is connected to a first terminal on a surface of said upper chip, a second terminal is connected to a terminal on a surface of said substrate, and said wiring pattern connects said second terminal to said terminal on a surface of said upper chip.

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Claim 3 (currently amended): A stacked semiconductor storage device as claimed in claim 2, further comprising a ~~second~~ bonding wire for connecting said terminal of the surface of said substrate with said second terminal.

Claim 4 (previously presented): A stacked semiconductor storage device as claimed in claim 1, wherein there is provided a wiring pattern whose one end is connected to a terminal on a rear surface of said upper chip, and whose other terminal is connected to a terminal on a surface of said lower chip.

Claim 5 (previously presented): A stacked semiconductor storage device as claimed in claim 2, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

Claim 6 (previously presented): A stacked semiconductor storage device as claimed in claim 4, wherein said terminal of the surface of said lower chip is connected to said terminal of the surface of said substrate by a third bonding wire.

Claim 7 (previously presented): A stacked semiconductor storage device as claimed in claim 1, wherein said wiring substrate is a sheet wiring substrate.

Claim 8 (previously presented): A stacked semiconductor storage device as claimed in claim 1, wherein said wiring substrate is a board wiring substrate.

Claim 9 (currently amended): A semiconductor device, comprising:

a package substrate having a first pad;

a first chip having a second pad and formed on said package substrate;

a wiring substrate formed on said first chip, said wiring substrate having a third pad, a

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fourth pad and a wiring pattern connected between said third and fourth pads; and

a second chip having a fifth pad and formed on said ~~second chip~~ wiring substrate;

a first bonding wire connecting said first pad and said third pad; and

a second bonding wire connecting said fourth pad and said fifth pad.

Claim 10 (canceled)

Claim 11 (currently amended): The semiconductor device as claimed in claim [[10]] 9, wherein no bonding wire connects said first pad and said fifth pad.

Claim 12 (currently amended): [[The]] A semiconductor device ~~as claimed in claim 9,~~ comprising:

a package substrate having a first pad;

a first chip having a second pad and formed on said package substrate;

a wiring substrate formed on said first chip, said wiring substrate having a third pad, fourth pad and a wiring pattern connected between said third and fourth pads, and

a second chip having a fifth pad and formed on said wiring substrate, wherein ~~one of~~ said third pad ~~and said fourth wiring pattern~~ is in direct contact with ~~one of~~ said second pad ~~and fifth pads~~.

Claim 13 (currently amended): The device as claimed in claim [[10]] 9, said device further comprising a third bonding wire connecting said first pad, wherein said third bonding wire and said first bonding wire are connected with the same first pad.

Claim 14 (currently amended): ~~A semiconductor~~ The device as claimed in claim 12, said device comprising:

a package substrate having a plurality of first pads;

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a first chip having a plurality of second pads and formed on said package substrate;

a wiring substrate formed on said first chip, said wiring substrate having a plurality of third pads, a plurality of fourth pads and ~~a plurality of~~ wiring patterns connected between said third and~~, each of said wiring patterns connecting a corresponding one of said third pads and a corresponding one of said~~ fourth pads; and

a second chip having a plurality of fifth pads and formed on said ~~second chip~~ wiring substrate; wherein ~~said fourth pads are connected to said fifth pads, said first pads are connected to said second pads, and a first wiring is provided to connect said first pads and~~ said third pads are in direct contact with said second pads.

Claim 15 (previously presented): The semiconductor device as claimed in claim 14, wherein one of said first pads is connected to one of said second pads as well as one of said third pads.

Claim 16 (currently amended): A stacked semiconductor storage device as claimed in claim [[9]] 12, wherein said wiring substrate is a sheet wiring substrate.

Claim 17 (currently amended): A stacked semiconductor storage device as claimed in claim [[17]] 12, wherein said wiring substrate is a board wiring substrate.

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